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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,417	08/15/2003	Hung-Jen Chu	38699-8033US	1459

25096 7590 11/08/2005

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EXAMINER	
NOVACEK, CHRISTY L	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/642,417	CHU ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed August 30, 2005.

Response to Amendment

The amendment of claim 18 is sufficient to overcome the rejection of claim 18 under 35 U.S.C. 112, second paragraph stated in the previous office action. Therefore, this rejection is withdrawn.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of West et al. (US 6,521,975, previously cited).

Regarding claim 13, the admitted prior art discloses providing a first substrate, forming a gate electrode and a gate electrode line on the substrate, wherein the gate electrode line includes a gate terminal and a lead, depositing a blanket gate insulating layer on the gate electrode, gate electrode line, and substrate, forming an island semiconductor layer on the gate electrode and a source electrode and a drain electrode on the island semiconductor layer, and depositing a blanket passivation layer on the source electrode, the drain electrode (Fig. 1; para. 0004-0006). The admitted prior art discloses a scribing line located at the periphery of the gate electrode line on a margin of a second substrate with a color filter thereon, but does not disclose forming a resist region located at the scribing line. Like the admitted prior art, West discloses a process of forming an integrated circuit device on a substrate, wherein the substrate and overlying layers are

subjected to a scribing process to divide the substrate into individual integrated circuits. West teaches that the overlying layers on the substrate are prone to cracking under the strain imposed by the scribing process (col. 3, ln. 36 – col. 4, ln. 50). To prevent the cracking from destroying the integrated circuit, West teaches that it is beneficial to deposit a resist region at the scribing line over the integrated circuitry on the substrate (col. 4, ln. 56-62). West states that these resist regions can be deposited and patterned at the same time as other metal layers in the integrated circuit (col. 7, ln. 33-35). At the time of the invention, it would have been obvious to one of ordinary skill in the art to deposit the resist regions of West over the gate electrode line and terminal and at the scribe region of the admitted prior art because West discloses that these resist regions are beneficial when used in any type of integrated circuit that is being diced and because West teaches that these resist regions can prevent crack propagation from destroying the integrated circuit.

Regarding claim 14, West discloses that the resist regions are made of metal (col. 4, ln. 56-62).

Regarding claim 15, West discloses that the resist region can be floating (col. 9, ln. 56 – col. 10, ln. 11).

Regarding claim 16, as stated above, West discloses that the step of formation the metal resist region can occur simultaneously with any metal feature formation step.

Regarding claim 17, the admitted prior art discloses forming an island semiconductor layer on the gate insulating layer and over the gate electrode, depositing a blanket metal layer on said island semiconductor layer and the gate insulating layer, performing a lithographic process to the conductive layer by using a reticle with a source pattern and a drain pattern on the gate

electrode and etching the conductive layer to form the source and drain electrodes. West discloses that the step of formation the metal resist region can occur simultaneously with any metal feature formation step.

Regarding claim 18, the admitted prior art discloses that the gate electrode is a part of an active device thin-film transistor. West discloses that the resist region is dummy metallization that is not actively used in the integrated circuit. Therefore, the gate electrode line is more active than the resist region.

Regarding claim 19, West does not disclose any particular distance between the scribing line and the margin of the floating metal resist region. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use routine experimentation to determine an optimum distance between the scribing line and the margin of the resist region, depending upon the materials and thicknesses of the overlying layers and the method of scribing used, because West does not disclose any particular distance and because such variables of art recognized importance are subject to routine experimentation and discovery of an optimum value for such variables is obvious. See *In re Aller*, 105 USPQ 233 (CCPA 1955).

Regarding claim 20, West discloses that the width of the metal resist region can be about 0.2-0.6 micrometers. Neither West nor the admitted prior art discloses the width of the gate electrode line. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use routine experimentation to determine an optimum relative thickness between the resist region and the gate electrode line, depending upon the materials and thicknesses of the overlying layers and the method of scribing used, because neither West nor the admitted prior art disclose any particular relative thickness and because such variables of art recognized

importance are subject to routine experimentation and discovery of an optimum value for such variables is obvious. See *In re Aller*, 105 USPQ 233 (CCPA 1955).

Response to Arguments

Applicant's arguments filed August 30, 2005 have been fully considered but they are not persuasive.

Regarding the rejection of claim 13 as being unpatentable over the admitted prior art in view of West, Applicant argues that West does not disclose a resist region located at a scribing line. Claim 1 of West recites:

> "an array of integrated circuit chips bordered by scribe streets and separated by dicing lines;
> at least two sets of substantially parallel structures **within** each of said scribe streets, each set extending along the edge of a chip on opposite sides of each said dicing line, respectively;
> each of said sets comprising:
> at least one continuous barrier wall adjacent each chip, respectively; and
> at least one sacrificial composite structure in combination therewith, **between said wall and the center of said dicing line**, said composite structure being a discontinuous barrier wall comprising metal rivets interconnecting electrically conductive layers in an alternating pattern, whereby said composite structure provide mechanical strength to said sets and simultaneously disperses the energy associated with crack propagation." (emphasis added)

Therefore, West discloses that the resist region(s) are located at the scribing line. And by stating that the resist region can be located anywhere between the barrier wall in the scribe street and "the center of the dicing line", West acknowledges that the resist regions can be in the scribing line. In their remarks, Applicants assert, "As set forth in Claim 13, such resist layer is placed *right beneath* the scribing line". This is incorrect, as claim 13 recites no limitations that the resist region is "right beneath the scribing line." Instead, claim 13 recites that, "said resist region covers said gate terminal and said lead and is located at a scribing line".

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Morita et al. (US 5,414,297), Zommer (US 4835,592) and Smith et al. (US 4,364,078) disclose forming metal resist regions in scribing lines of semiconductor wafers.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
November 2, 2005